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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/659,872	09/13/2000	Hartmund Terletzki	00P7882US	7001

7590 12/05/2001

Siemens Corporation
Intellectual Property Department
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EXAMINER	
NGUYEN, MINH T	
ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 12/05/2001

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/659,872	TERLETZKI ET AL.	
	Examiner	Art Unit	
	Minh Nguyen	2816	

-- Th MAILING DATE of this communication app ars on th cover she t with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-6 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-6 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 20 July 2001 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☒ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Oath/Declaration

1. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP § 602.01 and 602.02.

The oath or declaration is defective because non-dated alterations have been made to the residence and post office address of the oath or declaration. See 37 CFR 1.52(c). Also, the box "Date" in the second inventor section is empty.

Drawings

2. The drawings are objected to because:

(i) the input transistor shown in Fig. 2 of the formal drawing submitted on 7/20/01 is mislabeled, i.e., "H1" should be changed to --N1--.

(ii) the grouping of the level shifting section and the enable/disable section shown Fig. 2 is not consistent with the specification (page 4, lines 21-22) and claim 2, i.e., the switching transistors P3 and N3 should be in the level shifting section.

Correction is required.

Specification

3. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The abstract of the disclosure is objected to because (i) it contains more than 150 words, (ii) it uses phrase which can be implied, i.e., "is provided" on line 11.

Correction is required. See MPEP § 608.01(b).

Claim Objections

4. Claims 1, 3 and 6 are objected to because of the following informalities:

As per claim 1, the claim has more than one period which is not complied with the requirement stated in MPEP 608.01(m). The term "input signal" recited on line 9 should be changed to --input logic signal-- to be consistent with the term used on line 2.

As per claim 3, "the enable/disable circuit" recited on line 1 should be changed to "the enable/disable section" to be consistent with the term used on line 7 of claim 1.

As per claim 6, "placing" recited on line 4 should be changed to --place--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 1, the claim is rejected as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: the recited enable/disable section does not have any structural relationship with the recited level shifting section in order for the enable/disable section to perform the function recited on lines 8-9. The recited "junction" on line 11, "first switching transistor" on line 12, "input transistor" on line 13, and "source of the third voltage level" on line 12 lack antecedent basis. The recitation "a first electrode coupled to the source of the third voltage level" on lines 12 is misdescriptive because it is clear that the recited output terminal provides the signal which has a third voltage level but certainly this output terminal cannot be a source to provide the third voltage level to the first electrode of the additional transistor as recited.

As per claim 2, "input transistor" recited on line 3 lacks clear antecedent basis because it is not clear if it is referring to the input transistor recited on line 13 of claim 1, "a source of the third voltage level" recited on line 8 lacks clear antecedent basis because it is not clear if it is referring to the source of the third voltage level recited on line 12 of claim 1 or another different

source which also provides the third voltage level, "junction" recited on line 10 lacks clear antecedent basis because it is not clear if this is referring to the junction recited on line 11 of claim 1, the "second voltage level" recited on line 14 lacks clear antecedent basis, i.e., it is not clear if this is referring to the second voltage level recited on line 3, and further, if it is related, it is not clear if the recitation "a second electrode coupled to the second voltage level" on line 13-14 means the second electrode is connected to receive the input logic signal since the input logic signal provides the second voltage level.

As per claim 4, the recitation "source of the first voltage level" on line 2 is unclear, i.e., it is not clear if there is any relationship between this source and the source which provides the input logic signal since the input logic signal also has the first voltage level.

As per claims 2-6, these claims are also rejected because of the indefiniteness of claim 1.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 4,216,390 to Stewart.

Stewart discloses a level shifting circuitry (Fig. 1) comprising:

a level shifting section 12 responsive to an input logic signal (the input signal at node 20) having a first voltage level (V2) representative of a first logic state "1" and a second voltage

level (V1) representative of a second logic state "0", and providing an output logic signal (the signal at node 30) at an output terminal 30 having a third logic voltage level (V3);

an enable/disable section 16 responsive to an enable/disable signal Vc for placing the output terminal 30 to a high output impedance condition (when transistor P3 is OFF) independent of the logic state of the input signal during a disable mode;

wherein the level shifting section includes an additional transistor P26 having a control electrode connected to the junction (node 30), a first electrode connected to a source having a third voltage level V3 through a first switching transistor P3 and a second electrode connected to the second electrode of an input transistor N3 (node 28) and wherein the input transistor N3 and the additional transistor P26 are of opposite conductivity type.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 4,216,390 to Stewart.

As per claim 2, Stewart discloses a level shifting circuitry (Fig. 1) comprises elements and connections as discussed in claim 1 above wherein the level shifting section includes:

an input transistor N3 having a first electrode 22 coupled to the input logic signal 20;

a first switching transistor P3;

an output pair complementary transistors P1b and N1b wherein P1b having a first electrode 34 coupled to the source of the third voltage level V3 through the first switching transistor P3, a control electrode coupled to the second electrode of the input transistor N3 at node 28, a junction 30 and wherein the control electrode of N1b is coupled to the first electrode of the input transistor N3 through diode D1 and the second electrode of the second one of the output transistors N1b is directly coupled to ground.

Stewart does not explicitly teaches the level shifting section in Fig. 1 further includes a second switching transistor N3 and the second one of the pair transistor having a second electrode coupled to a source of a second voltage level through the second switching transistor as called for in the claim.

Stewart discloses another level shifting circuit (Fig. 3) having a second switching transistor N5A, and he further teaches that when the input logic signal swings in a negative region (column 4, line 31), i.e., the second voltage level is negative, a second switching transistor N5A should be added (column 4, lines 30-60).

It would have been obvious to one skilled in the art at the time of the invention was made to include a second switching transistor taught in Fig. 3 of the Stewart reference to the Stewart's level shifting section shown in Fig. 1.

The motivation/suggestion for doing so would have been to allow the Stewart's level shifting circuit shown in Fig. 1 to function when the levels of the input logic signal is either positive or negative.

Therefore, it would have been obvious to add the second switching transistor to Fig. 1 of the Stewart reference to obtain the invention as specified in claim 2.

As to the limitation that the first and second switching transistors are fed by the enable/disable signal. This limitation would have been obvious also since the first and second switching transistors must be both ON or OFF during any period of time, therefore, by using only one signal, this requirement can be obtained. A further motivation would have been by using a single signal, the control section would be simpler.

As per claim 3, the recited limitation that the enable/disable section includes an inverter is inherently met because as shown in Fig. 1 and 3, the first switching transistor P3 is P type and the second switching transistor N5A is N type, therefore, when using only the enable/disable signal to turn ON or OFF both of these transistor, an inverter must be included.

As per claim 4, since it is clear that the inverter discussed in claim 3 above must be powered by a voltage source, the recited "source of the first voltage level" reads on the voltage source which provides the power for the inverter.

As per claim 5, the combination discussed in claim 4 above discloses that the control electrode of the input transistor N3 is coupled to a source having a voltage level V2 as shown in Fig. 1 of the Stewart reference but does not explicitly disclose that this source is the same as the source providing the power for the inverter. However, it is old and well-known that it is desirable to use a same source to supply power for a circuit because it is more convenience and it requires less space. It would have been obvious to one skilled in the art at the time of the invention was made to use the same source to provide the power for the control electrode of the input transistor and the inverter for the obvious advantage discussed herein above.

Allowable Subject Matter

8. Claim 6 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Claim 6 is allowable because the prior art of record fails to disclose or suggest a level shifting circuit which includes a level shifting section and an enable/disable section wherein the enable/disable section includes an inverter which comprises a level shifter circuit for shifting the enable/disable signal from a first voltage level to a third voltage level as recited in the claim.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Patent No. 4,656,373 to Plus discloses a level shifting circuit (Fig. 3) which includes a level shift section 12, an enable/disable section 16.

US Patent No. 5,723,987 to Ronen discloses a level shifting circuit (Fig. 1) which includes switching transistors 14 and 17, a pair of output transistors 15 and 16 and enable/disable control signal EN.

US Patent No. 5,748,024 to Takashashi et al discloses a level shifting circuit (Fig. 4) which includes inverter 11, switching transistors 21 and 24 and output transistors 22 and 23.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is 703-306-9179. The examiner can normally be reached on Monday - Thursday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Minh Nguyen
Examiner
Art Unit 2816

November 23, 2001